

■ GENERAL DESCRIPTION

The AS5430 is a monolithic synchronous buck regulator. The device integrates 100mΩ MOSFETS that provide 3A continuous load current over a wide operating input voltage of 4.75V to 23V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An adjustable soft-start prevents inrush current at turn-on. In shutdown mode, the supply current drops below 1μA. The device provides a very compact system solution with minimal reliance on external components.

■ FEATURES

- ◆ 3A Output Current
- ◆ Integrated 100mΩ Power MOSFETS
- ◆ Wide 4.75~23V Input Voltage Range
- ◆ Programmable Soft-start
- ◆ Up to 95% Efficiency
- ◆ Stable with Low ESR Ceramic Output Capacitors
- ◆ Output Adjustable From 0.925V to 20V
- ◆ Cycle-by-Cycle Over Current Protection
- ◆ Input Under Voltage Lockout
- ◆ Fixed 400KHz Frequency

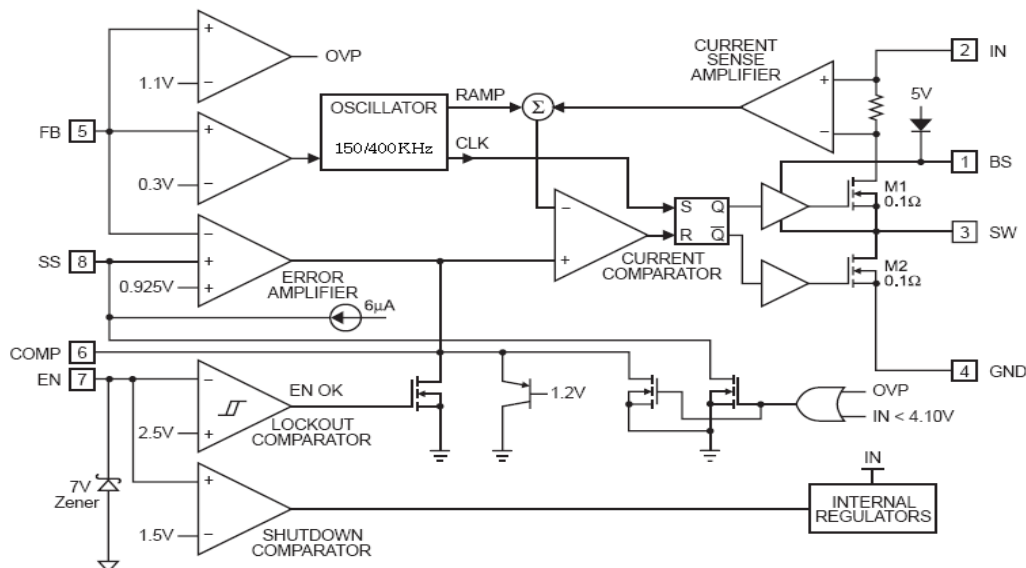
■ APPLICATION

- ◆ Distribute Power Supply
- ◆ Networking Systems
- ◆ Notebook or Mini-book
- ◆ LCD TV/LCD Monitor

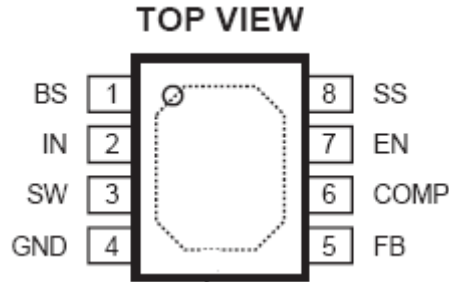
■ ORDER INFORMATION

| Order Number | Package | Packing | Remark |
|---------------|-------------------|---------------------|-----------|
| AS5430D/TR-LF | SOP8(Exposed Pad) | Tape&Reel, MPQ=2500 | Lead-Free |

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

| Pin# | Name | Description |
|------|------|---|
| 1 | BS | High-side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01uF or greater capacitor from SW to BS to power the high-side switch |
| 2 | IN | Power Input. Input with a 4.75~23V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. |
| 3 | SW | Power Switching Output. Switching mode that supplies power to the output. Connect the output LC filter from SW to the output load. |
| 4 | GND | Ground, connect Exposed Pad to Pin4 |
| 5 | FB | Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. |
| 6 | COMP | Compensation mode. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. |
| 7 | EN | Enable Input. EN is digital input that turns the regulator on or off. Drive EN high to turn on the regulator. Drive it low to turn it off. Pull up with 100K ω resistor for automatic startup. |
| 8 | SS | Soft-start control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.01uF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected. |

ABSOLUTE MAXIMUM RATING^(Note1)

| | |
|----------------------------------|------------------------------|
| Input Voltage, V_{IN} | -0.3V to 26V |
| Switch Voltage, V_{SW} | -1V to $V_{IN}+0.3V$ |
| Bootstrap Voltage, V_{BS} | $V_{SW}-0.3V$ to $V_{SW}+6V$ |
| Enable/UVLO Voltage, V_{EN} | -0.3V to 6V |
| Comp Voltage, V_{comp} | -0.3V to 6V |
| Feedback Voltage, V_{FB} | -0.3V to 6V |
| Storage Temperature Range, T_S | -55°C to 150°C |
| Lead Temperature | 260°C |
| Junction Temperature, T_J | 150 °C |

OPERATION RATING^(Note2)

| | |
|--------------------------|----------------|
| Input Voltage, V_{IN} | 4.75V to 23V |
| Output Voltage, V_{SW} | 0.925V to 20V |
| Operation Temperature | -20°C to +85°C |

THERMAL RESISTANCE^(Note3)

| | |
|----------------------|--------|
| SOIC8, θ_{JA} | 50°C/W |
| SOIC8, θ_{JC} | 10°C/W |

ELECTRICAL CHARACTERISTICS^($V_{IN}=12V, T_A=+25^\circ C$, unless otherwise noted)

| Parameter | Test Conditions | Min | Typ | Max | Units |
|--|-----------------------------------|-----|-----|-----|------------|
| Shutdown Supply Current | $V_{EN} \leq 0.3V$ | | 0.3 | 3.0 | μA |
| Supply Current | $V_{EN} \geq 2.6V, V_{FB} = 1.0V$ | | 1.3 | 1.5 | mA |
| Feedback Voltage | $4.75V \leq V_{IN} \leq 23V$ | 900 | 925 | 950 | mV |
| Feedback Overvoltage Threshold | | | 1.1 | | V |
| Error Amplifier Voltage | | | 480 | | V/V |
| Error Amplifier Transconductance | $\Delta I_C = \pm 10\mu A$ | | 800 | | $\mu A/V$ |
| High-side Switch-On Resistance | | | 100 | | m Ω |
| Low-side Switch-On Resistance | | | 100 | | m Ω |
| High-side Switch Leakage | $V_{EN} = 0V, V_{SW} = 0V$ | | 1 | 10 | μA |
| Upper Switch Current Limit | | 4.0 | 6.0 | | A |
| Lower Switch Current Limit | | | 0.9 | | A |
| COMP to Current Sense Transconductance | | | 5.2 | | A/V |
| Oscillator Frequency | | 350 | 400 | 450 | KHz |
| Short Circuit Frequency | $V_{FB} = 0V$ | | 150 | | KHz |
| Maximum Duty Cycle | $V_{FB} = 0.8V$ | | 90 | | % |
| Minimum On Time | | | 120 | | nS |
| EN Shutdown Threshold Voltage | V_{EN} Rising | 1.1 | 1.5 | 2.0 | V |
| EN Shutdown Threshold Voltage Hysterisis | | | 200 | | mV |
| EN Lockout Threshold Voltage | | 2.2 | 2.5 | 2.7 | V |

■ ELECTRICAL CHARACTERISTICS (CONTINUOUS)

| Parameter | Test Conditions | Min | Typ | Max | Units |
|-------------------------------------|-------------------|------|------|------|-------------|
| EN Lockout Hysterisis | | | 210 | | mV |
| Input UVLO Threshold Rising | V_{IN} Rising | 3.80 | 4.20 | 4.40 | V |
| Input UVLO Threshold Hysteresis | | | 210 | | mV |
| Soft-start Current | $V_{SS}=0V$ | | 6.5 | | μA |
| Soft-start Period | $C_{SS}=0.1\mu F$ | | 15 | | ms |
| Thermal Shutdown ^(Note4) | | | 160 | | $^{\circ}C$ |

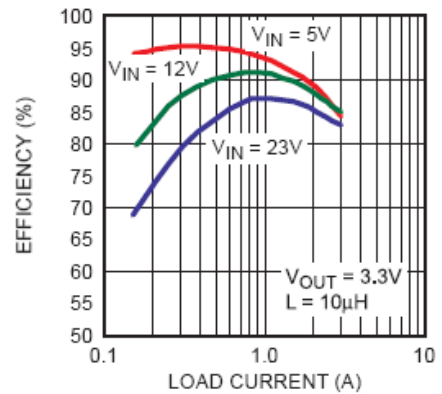
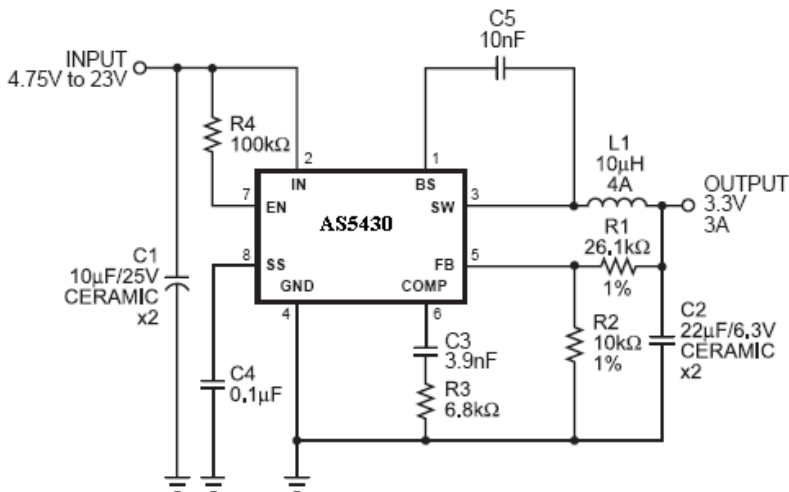
Note1: Exceeding these rating may damage the device.

Note2: The device is not guaranteed to function outside of its operation conditions

Note3: Measured on approximately 1" square of 1 oz copper.

Note4: Guaranteed by design.

■ TYPICAL APPLICATION



■ DETAILED DESCRIPTION

Functional Description

The AS5430 is a synchronous rectified, current - mode, step-down regulator. It regulates input voltage from 4.75V to 23V down to an output voltage as low as 0.925V, and supplies up to 3A of load current.

The AS5430 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier. The voltage at the COMP pin is compared to the switch current measured internally to control the output voltage.

Application Information

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB. The voltage divider the output voltage down by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1 + R2}$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage. Thus the output voltage is:

$$V_{OUT} = 0.925 \times \frac{R1 + R2}{R2}$$

$R2$ can be as high as 100k Ω , but a typical value is 10k Ω . Using the typical value for $R2$, $R1$ is determined by:

$$R1 = 10.81 \times (V_{OUT} - 0.925) \text{ (k}\Omega\text{)}$$

For example, for a 3.3V output voltage, $R2$ is 10k Ω , and $R1$ is 26.1k Ω . Table 1 lists recommended Resistance values of $R1$ and $R2$ for standard output voltage

Table1--Recommended Resistance Values

| V_{out} | $R1$ (k Ω) | $R2$ (k Ω) |
|-----------|--------------------|--------------------|
| 1.8V | 9.53 | 10 |
| 2.5V | 16.9 | 10 |
| 3.3V | 26.1 | 10 |
| 5V | 44.2 | 10 |
| 12V | 121 | 10 |

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the AS5430 FB pin exceeds 20% of the nominal regulation voltage of 0.925V, the over voltage comparator is tripped and the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

INDUCTOR

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_s is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Where I_{LOAD} is the load current. The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI requirements.

OPTIONAL SCHOTTKY DIODE

During the transition between high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency. Table2 lists example schottky diodes and their manufacturers.

Table2—Diode Selection Guide

| Part# | Voltage/Current Rating | Vendor |
|---------|------------------------|-------------------------|
| B130 | 30V,1A | Diodes |
| SK130 | 30V,1A | Diodes |
| MBRS130 | 30V,1A | International Rectifier |

INPUT CAPACITOR

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors. Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{in}=2V_{OUT}$, where $I_{CIN}=I_{LOAD}/2$. For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum or capacitors, a small, high quality ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input

Voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C1 \times f_s} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where C1 is the input capacitance value.

OUTPUT CAPACITOR

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right)$$

Where C2 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The AS5430 optimized for a wide range of capacitance and ESR values.

COMPENSATION COMPONENTS

AS5430 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{OUT}}$$

Where V_{FB} is the feedback voltage 0.925V; A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor(C3) and the output resistor of the error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where G_{EA} is the error amplifier transconductance. the system has one zero of importance, due to the compensation capacitor(C3) and the compensation resistor(R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance If the output capacitor has a large capacitance and /or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor(C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good rule of thumb is to set the crossover frequency below one-tenth of the switching frequency. To optimize the compensation components, the

Following procedure can be used.

1. Choose the compensation resistor(R3) to set the desired crossover frequency. Determine the R3 value by the following equation:

$$R3 = \frac{2\pi \times C2 \times f_c}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} < \frac{2\pi \times C2 \times 0.1 \times f_s}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_c is the desired crossover frequency which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor(C3) to Achieve the desired phase margin. For application With typical inductor values, setting the compensation zero, f_{Z1} , below one-fourth of the cross-over frequency provides sufficient phase margin. Determine the C3 value by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_c}$$

Where R3 is the compensation resistor.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the Output capacitor is located at less than half of the Switching frequency, or the following relationship is Valid:

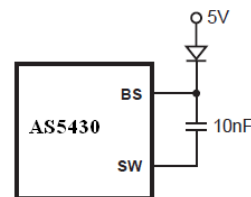
$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_s}{2}$$

If this is the case, then add the second compensation capacitor(C6) to set the pole f_{P3} at the location of the ESR zero. Determine the C6 value by The equation:

$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

EXTERNAL BOOTSTRAP DIODE

It is recommended that an external bootstrap diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.



This diode is also recommended for high duty cycle operation (when $\frac{V_{OUT}}{V_{IN}} > 65\%$ and output voltage $V_{OUT} > 12V$) applications.

TYPICAL APPLICATION CIRCUITS

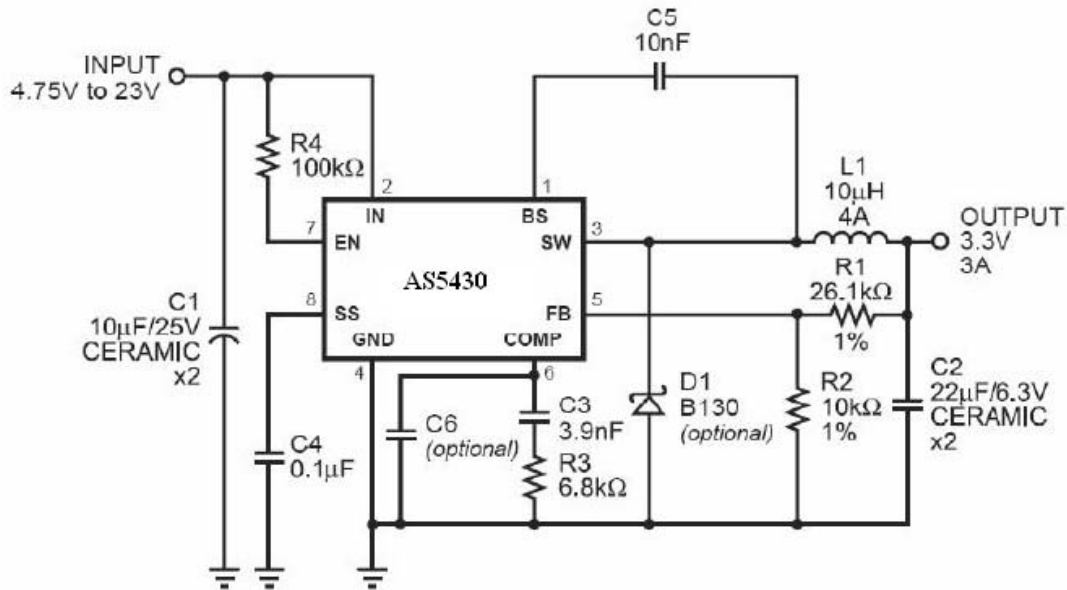


Figure 1----AS5430 with 3.3V output, 22uF/6.3V Ceramic Output Capacitor

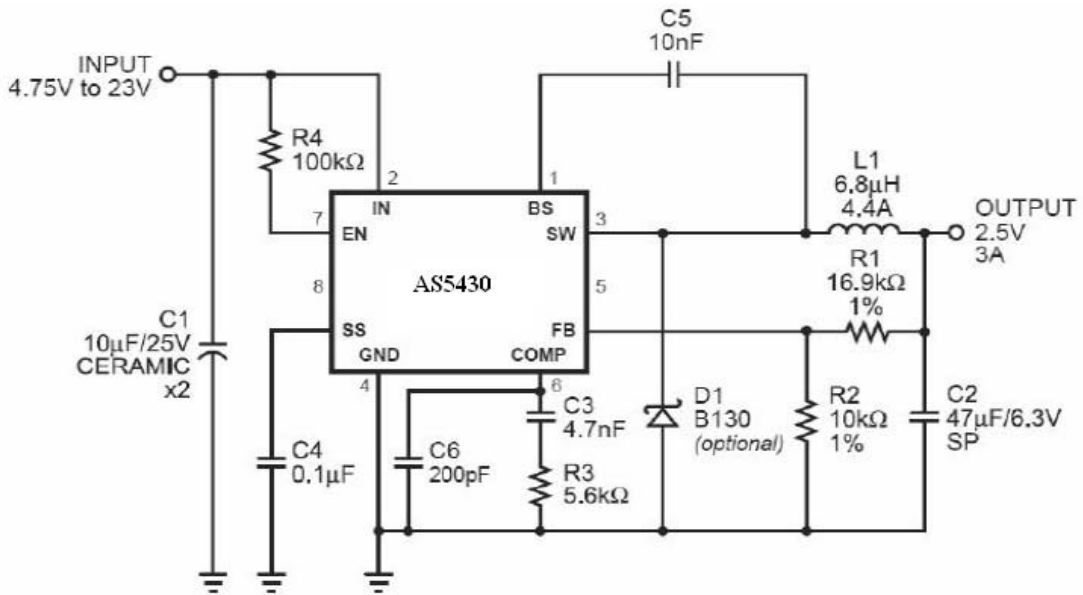
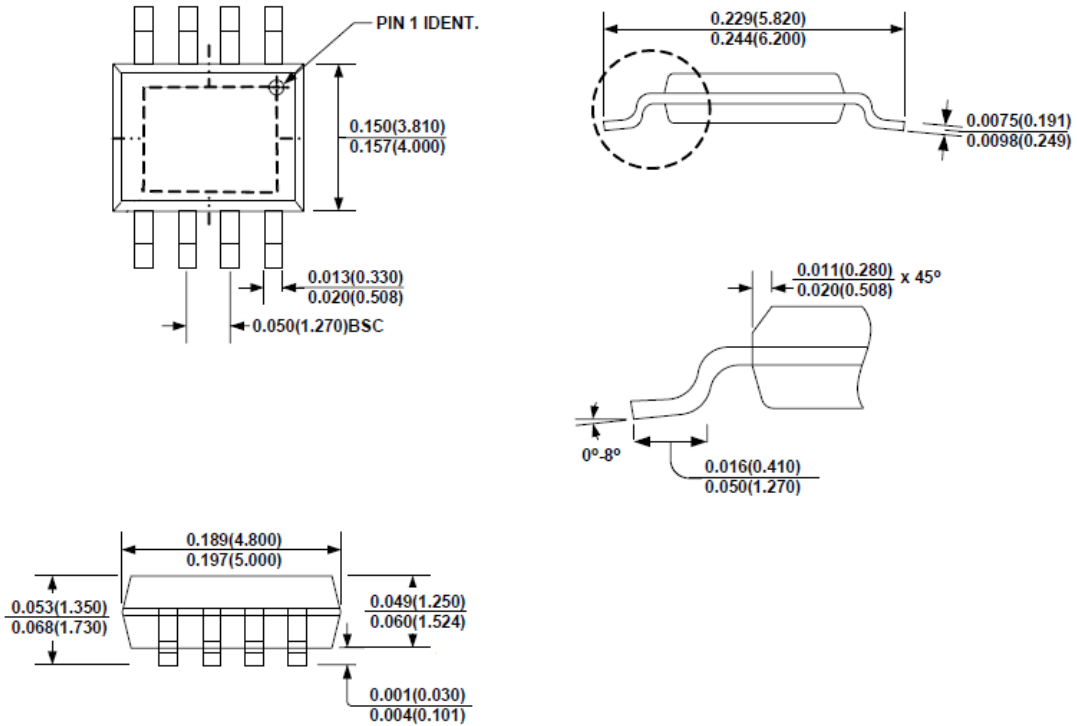


Figure 2----AS5430 with 2.5V output, 47uF/6.3V Ceramic Output Capacitor

PACKAGE INFORMATION

SOIC8N (EXPOSED PAD)



- _____:
- 1) Dimension in bracket is millimeters
 - 2) Exposed Pad Option: $2.55 \pm 0.25\text{mm} \times 3.38 \pm 0.44\text{mm}$
Recommended Solder Board Area: $2.80 \times 3.82\text{mm} = 10.7\text{mm}^2$