1. Features

Core

- ✓ 32-bit Arm® Cortex®-M3 Core
- ✓ Up to 72MHz working frequency, 1.25 DMIPS / MHz (Dhrystone 2.1) performance at 0 wait state memory access
- ✓ Single-cycle multiplication and hardware division

Memories

- ✓ 64 or 128 Kbytes of Flash memory
- ✓ 20 Kbytes of SRAM

Reset and power management

- ✓ 1.8 to 5.0 V application supply and I/Os
- ✓ POR, PDR, and programmable voltage detector (PVD)
- ✓ Low power modes: Sleep, Stop, Standby V_{BAT} supply for RTC and backup registers

Clock management

- ✓ 4 to 16 MHz crystal oscillator
- ✓ Internal 8 MHz factory-trimmed RC
- ✓ Internal 40 kHz RC
- ✓ 32 kHz oscillator for RTC with calibration

Peripheral features

- ■ 2 x 12-bit, 1μs ADC (up to 16 channels)
  - ✓ Conversion range: 0 to 5.0 V
  - ✓ Dual-sample and hold capability
  - ✓ Temperature sensor
- ■ DMA：7-channel DMA controller
  - ✓ Supported peripherals: timers, ADCs, SPIs, I2Cs and USARTs
- ■ Debug mode
  - ✓ Serial wire debug (SWD) & JTAG interfaces
- ■ Up to 80 fast I/O ports
  - ✓ 37/51/80 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant
- ■ Up to 7 timers
  - ✓ Three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - ✓ 16-bit motor control PWM timers with deadtime generation and emergency stop
  - ✓ 2 x watchdog timers (Independent and Window)
  - ✓ SysTick timer: a 24-bit downcounter
- ■ Up to 9 communication Interfaces
  - ✓ Up to 2 x I2C interfaces
  - ✓ Up to 3 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - ✓ Up to 2 SPIs (18 Mbit/s)
  - ✓ CAN interface (2.0B Active)
  - ✓ USB 2.0 full speed interface
- ■ CRC calculation unit, 96-bit unique ID
- ■ Packages : LQFP48, LQFP64, LQFP100